White Paper

Federal & Aerospace

Intel® and CoreAVI Avionic Solutions Using Intel Performance Hybrid Architecture

The introduction of advanced architectures has accelerated the transition to multi-core processors, bringing certification and validation challenges for avionics engineers who are building new solutions. The 13th Gen Intel® Core™ series of processors will greatly increase the advantages of a System-on-Chip (SoC) architecture that employs both "high performance" and "efficiency" cores. The two core types can run independently yet they share interfaces.

Interactive software systems with embedded safety features ensure the safety of the aircraft, passengers, and environment. Partnerships between cutting-edge software and hardware companies are also key to creating productive and more efficient certification processes for avionics engineers. CoreAVI has collaborated closely with Intel to port their best-in-class certifiable graphics and compute libraries to selected Intel processors. CoreAVI's graphics and image processing libraries support the Khronos Group's ratified Vulkan® SC™ standard, which allows avionics manufacturers to leverage Intel's integrated graphics processing unit (GPU) to handle graphics and image processing, as well as neural networking applications. Platform applications that require the exposure of low-level GPU operations for critical operations will find both real time and deterministic support to meet the demands of safety critical requirements, such as DO-178C/ED-12C and DO-254/ED-80.

Authors

Maurizio Iacaruso - Intel
Elisa Spano' - Intel
Laura Spinella - Intel
Ken Wenger - CoreAVI
Michael Pyne - CoreAVI

Table of Contents

Introduction

While multi-core processors (MCPs) have been widely used in all industry fields for many years, MCPs with only one core enabled remain the avionic segment preferred choice, due to the complexity of MCP certification. Nevertheless, the growing need for compute power requirements and reduction in size, weight and power (SWaP) are pushing the full embrace of multi-core processors in safety-critical airborne software. Multi-core processors are candidates to become the preferred choice for the future generation of airborne embedded systems to satisfy processing performance requirements and SWaP reduction of digital electronic hardware in avionics.

However, flight safety certification is challenging because semiconductor manufacturers designing MCPs for the commercial market tend to optimize their processors for broad market performance, not safety and isolation. MCPs generally do not separate hardware resources per core. Instead, they employ more shared resources and out-of-order processors, and they don't provide robust partitioning. Nevertheless, MCPs can be used to build safety certifiable systems. This is done by identifying and mitigating interferences and determining the worst-case execution time of a thread by analysis and confirming by test. Silicon suppliers and their software partners assume a key role by providing pre-integrated solutions to enable the certification processes to be more efficient.

Avionics certification requires extensive verification of software and hardware to ensure the safest operation. Software systems with pre-integrated safety certifiable solutions such as board support packages (BSPs) and graphics drivers can allow more efficient certification processes of the fully integrated system. Avionics hardware system developers also need significant design assurance data from silicon vendors to develop their certification evidence packages.

This white paper provides a brief introduction to Intel's performance hybrid architecture and discusses how this architecture combined with CoreAVI's certifiable graphics and compute products and the Intel® Airworthiness Evidence Package can be used to develop flexible, high-performance, certifiable solutions for safety-critical avionics applications.

Intel performance hybrid architecture

Intel's performance hybrid architecture merges two existing architectures: Performance-cores (P-cores) and Efficiency-cores (E-cores). These two architectures complement each other to deliver the best possible experience to customers and end-users. Single and multiple-threaded operations are performed simultaneously, despite the constraints dictated by the power capacities and other equipment limitations. By having both P-cores and E-cores, Intel's performance hybrid architecture can generate a more efficient distribution of core usage depending on the application. This happens because P-cores help increase performance to handle complex workloads (typically those with limited threading). E-cores meanwhile focus on multi-threaded throughput and power-limited scenarios.

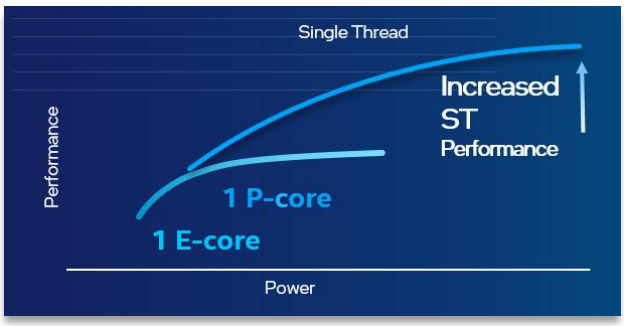

Figure 1:Single-thread power and performance characteristics on P-core and E-core

Certain workloads can be bound to certain cores. As shown in Figure 1, a P-core provides more performance compared to an E-core at higher power envelopes. At lower power envelopes, E-cores have better performance than P-cores. Generally, the P-cores are preferred for priority tasks and limited threading applications, while the E-cores are available to perform in power-limited scenarios and/or background applications that can meet their Quality of Service (QoS) requirements on that performance. Intel's performance hybrid architecture has P-cores and E-cores working alongside one another. This creates an exciting opportunity because this architecture can work well on single-threaded or partially threaded applications as well as multi-threaded applications.

Performance hybrid architecture and avionics use cases

Electronic systems on aerospace platforms require extensive safety and reliability considerations. To ensure safety for pilots, crews and passengers, system architectures and hardware and software components are conceived, designed, tested, validated, and certified in a very rigorous fashion. Redundancy, the incorporation of disparate design elements, along with fault detection and handling become key elements in almost every safety critical aerospace system. Industry guidelines for the development of safety critical hardware and software for aerospace systems are documented in the standards, RTCA DO-178C/ED-12C: Software Considerations in Airborne Systems and Equipment and RTCA DO-254/ED-80, Design Assurance Guidance for Airborne Electronic Hardware.

Due to the great flexibility provided by Intel's performance hybrid architecture and CoreAVI's certifiable graphics and compute libraries, avionics use cases can be satisfied by several different silicon and software configurations. This allows Tier 1 and Tier 2 suppliers to propose different configurations to their customers using a single hardware baseline thus further reducing certification costs. One possible configuration that leverages the performance hybrid design can have P-cores assigned to lower criticality and high-performance tasks (e.g. graphics) with E-cores assigned to high criticality, lower power and highly deterministic tasks (e.g. safety monitoring). Additionally, an external safety island can be used to monitor the entire system, making decisions on failure handling and safe state management.

CoreAVI has ported VkCore® SC, a certifiable graphics and compute driver to Intel's architecture. VkCore® SC is designed for safety-critical applications, which is aligned with the new Vulkan SC API from the Khronos Group.

In addition, CoreAVI has developed a portfolio of software libraries, drivers, and safety monitoring applications that run on select Intel multi-core processors, support multi- level partitioning and mixed criticality levels, see Figure 2. These systems rely upon a real time operating system that processes data and events within preset time constraints and that support the partitioning of functions to different cores (and sometimes within a given core). This partitioning is generally robust in both resource and time domains. Typically, an instantiation of the operating system primary kernel runs on one of the P-cores within the SoC. Processor cores can be partitioned by the operating system or by a hypervisor. A one-to-one mapping between an operating system instantiation and a core is not necessary. In many cases, the hypervisor also allows for different 'guest' operating systems to run on selected cores.

In general, these systems employ asymmetric multiprocessing (rather than symmetric multiprocessing) which ensures that all

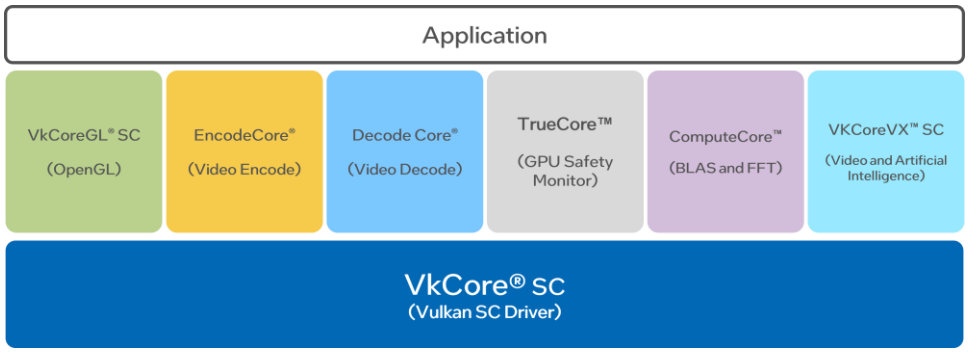

Figure 2: CoreAVI Vulkan Safety Critical Components

functional processes are allocated to a given core – sometimes called 'core affinity'.

These architectures are supported by using a safety certifiable real time operating system (RTOS) that guarantees proper core and resource partitioning to avoid and mitigate most known interferences, see Figure 3. Alternatively, a safety certifiable hypervisor, also known as kernel separation hypervisor, provides hardware separation among partitions running different operating systems on the platform, see Figure 4. As depicted in Figure 4, different operating systems and applications can have differing Design Assurance Levels (DAL), allowing use cases with mixed criticality running on the same platform.

The following use cases provide examples of safety-critical applications running on the architectures proposed in Figure 3 and Figure 4.

Use case 1: A "self-contained" smart display with one display surface. In this configuration E-cores run safety critical monitors and built-in tests while working in parallel with P- cores that run the graphic drivers, graphic libraries and rendering applications. This case demonstrates the CoreAVI graphics driver (VkCore SC) and libraries (VkCoreGL® SC1, VkCoreGL® SC2, VkCoreVX™ SC and ComputeCore™). Learn more about these products in the following pages. This architecture demonstrates a simple stack of components and products that capitalize on the features of heterogeneous cores working in conjunction with a real time operating system, graphics drivers and graphic libraries

Use case 2: Display processors, driving many displays, where E-cores run safety critical monitors and cross display checks while P-cores run the graphics. The E-cores make any decisions requiring fault handling, contingency display switch-over, or degraded mode operations. This architecture generally represents a more complex case of multiple or guest operating systems running on a virtualized platform (e.g. hypervisor) that takes advantage of the intimate connections of the E-core and P-core hardware structure.

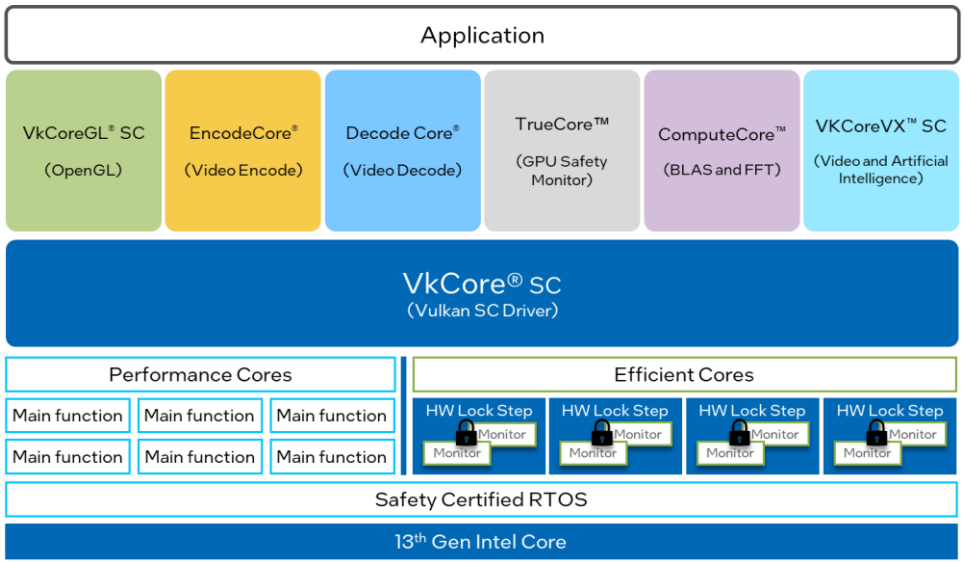

Figure 3: Native Software Architecture

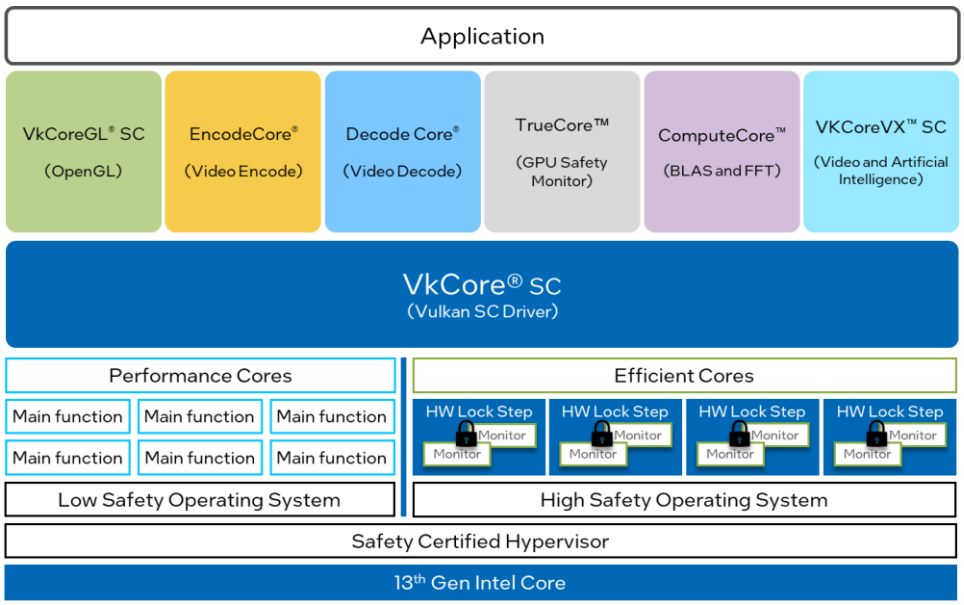

Figure 4: Virtualized Software Architecture

13th Gen Intel® Core™ processor and CoreAVI software portfolio

Intel's latest performance hybrid architecture product offering for the avionics market is the 13th Gen Intel® Core™ i7 processor with six P-cores for performance workloads and eight E-cores for low-power applications. Support for Instruction Set Architecture (ISA) has been adapted to the new architecture along with the most recent ISA updates and the 13th Gen Intel® Core™ processors have a common subset of ISA for both P- cores and E- cores further simplifying the porting of legacy applications to this new, power-efficient system.

13th Gen Intel® Core™ processors include a sophisticated Gen 12 Graphics Processing Unit (GPU), the Xe Graphics G7. This integrated GPU provides up to 96 graphics execution units allowing for a high degree of parallelization for AI workloads. The capabilities of this advanced GPU make it ideal not only for graphics but also for compute operations, such as executing neural networks and running other machine learning and artificial intelligence algorithms.

The 13th Gen Intel Core processor high-level block diagram is shown in Figure 5.

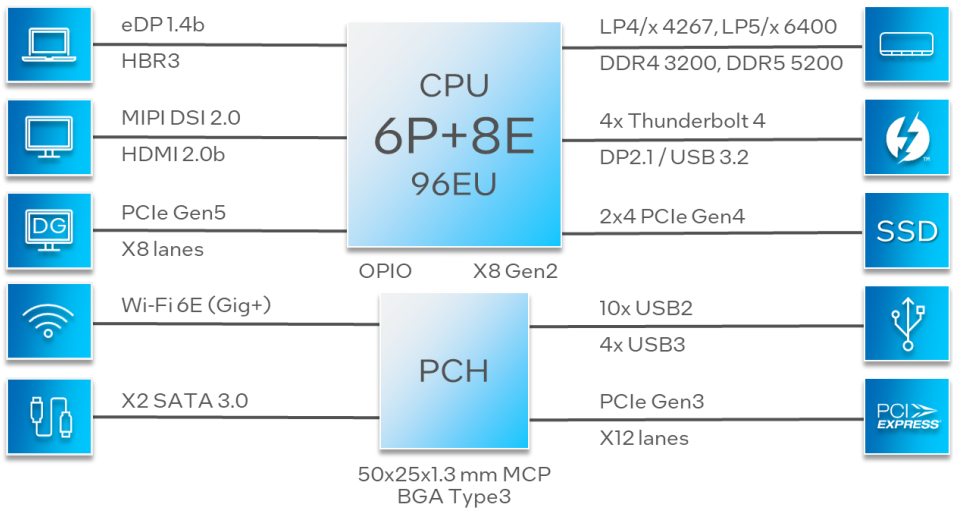

Figure 5: 13th Gen Intel Core processor high level block diagram

CoreAVI generally binds the Vulkan® SC driver onto one of the P-cores allowing applications running on different cores and at different safety levels to access the OpenGL® contexts needed to render graphics on cockpit displays. CoreAVI's OpenGL® SC™ libraries, called VkCoreGL® SC, can run on several guest operating systems simultaneously.

Besides graphics rendering applications, CoreAVI has developed a suite of functions and libraries for applications like video compression/decompression (EncodeCore®/ DecodeCore®) and for mathematical libraries (ComputeCore™) to support artificial intelligence and machine learning applications. These libraries include Basic Linear Algebra Subprograms (BLAS) and Fast Fourier Transformations (FFT) Application Programming Interfaces (APIs). The BLAS API enables the accelerated calculation of matrix and vector operations. A BLAS implementation is instrumental in most machine learning and signal processing ecosystems. The FFT API provides accelerated Fast Fourier Transformations used extensively in signal processing applications. For machine learning and deep-learning use cases, CoreAVI provides APIs for inferencing trained neural networks in a safety critical, deterministic manner (VkCoreVX™SC).

Determinism in multi-core processors

The majority of today's consumer or automotive SoCs include multi-core processor architecture, and the same is true in the aerospace market. However, multi-core processors present challenges to aerospace safety critical systems since the potential for conflict between resources may create threats to timing and determinism. The European Aviation Safety Agency (EASA) and the U. S. Federal Aviation Administration (FAA) have released separate guidelines for the use of multi-core processors in safety critical applications (i.e. EASA Certification Review and CAST-32A). These agencies are now working in concert to finalize these requirements in more formal use of multi-core processors in avionics applications and address component roles (processor architecture, operating system, drivers, etc.) along with approaches to modeling and testing such systems. To reduce the expense associated with software changes, the standard also allows for a 'mixed-criticality' approach that supports the classifying of different sections within the system at different safety criticality levels. If functional changes do occur, this approach allows for 'selective' re-verification, re- validation, and re- qualification rather than having to do wholesale testing of 'all' software components. CoreAVI works closely with component, operating system, and driver suppliers to ensure that these guidelines are properly followed.

One of the main drawbacks of multi-core architectures is the intrinsic presence of interference on the system due to shared resources. Shared resources can include memory controllers, system memory, I/Os, caches, and the internal fabric interconnect. An example of interference is the contention caused when multiple different processor cores try to access the same resources. This could prevent a high-criticality application from performing its intended functionality according to the required deadline. Understanding how critical time determinism is to safety-critical systems, Intel offers a 13th Gen Intel® Core™ i7 processor tailored for the avionics market that includes a set of features to address temporal requirement of avionics real-time applications, including:

- Silicon integrated features to minimize worst- case execution time, referred to as Intel® Time Coordinated Computing (Intel® TCC) features including Cache Allocation Technology (CAT),CPU/IO time synchronization, and memory bandwidth allocation.
- Disabled automatic thermal throttling to allow safety-critical applications full control over chip performance.
- AC/AMC 20-193 guidance included in the Intel® Airworthiness Evidence Package.
- Reference software Best Known Configurations (BKCs) with real-time optimizations.
- Software tools to accelerate hardware configuration/tuning and application development by enabling performance analysis and access to hardware features.

Certifying multi-core processors for safety critical applications

To help aerospace suppliers in their efforts to achieve certification, Intel licenses the Intel® Airworthiness Evidence Package (Intel® AEP) for select 13th Gen Intel Core processors. The Intel® AEP (Figure 6) is a collection of documents for DO-254 and ED-80 that aids in meeting the design assurance requirements of safety critical systems including flight control, cockpit display and flight monitoring systems. This enables Intel's customers to reduce time to market and deliver certifiable high- performance components.

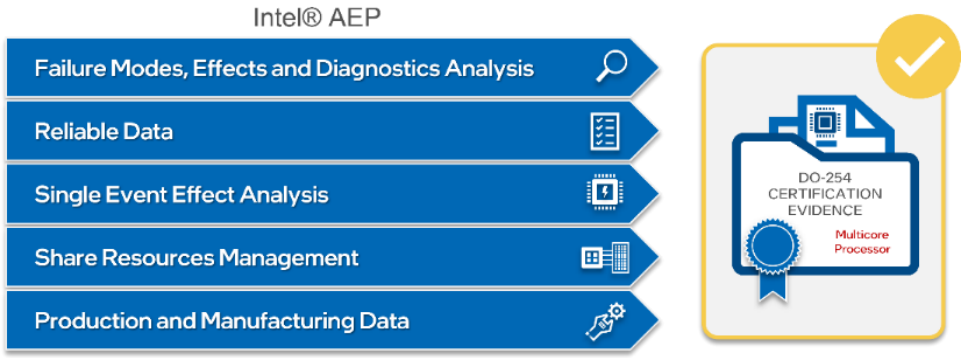

Figure 6: Intel® Airworthiness Evidence Package

Additionally, 13th Gen Intel® Core™ processors include several integrity features designed to detect hardware random failures at runtime, such as when a safety-critical application is executing. The main hardware integrity features are:

- Hardware Dual Core Lock Step (DCLS) provides the ability to configure two instances of E-cores to execute identical code and check the equivalence of outputs. This helps increase the reliability of the SoC.
- Parity/ECCs on the main arrays and register files of both P-cores and E-cores automatically detect two-bit errors and correct single-bit errors.
- End-to-end parity on the silicon fabric for high data integrity protection
- Power and clock monitoring
- Power on/power off diagnostic tests to detect latent faults

CoreAVI is intimately involved with the testing and safety certification of the drivers, libraries, and applications to the highest level of RTCA DO-178C and ED-12C. CoreAVI also does in-house hardware development and works with customers that use the Intel® AEP to significantly simplify the DO-254 certification process. CoreAVI's development team follows the intensive process rigor required by both DO-254/ED-80 and DO-178C/ED-12C. This includes software planning, development, verification, independent reviews, and structural coverage analysis. All these processes and procedures are audited by a third-party FAA Designated Engineering Representative (DER).

Conclusion

The partnership between Intel and CoreAVI is focused on delivering pre-integrated hardware and software solutions that bring confidence and accelerate time to market and certification. These solutions include Intel processors tailored for avionics, Intel-based hardware reference designs, certifiable RTOSes, middleware, CoreAVI software components and Intel® AEPs, which help aerospace suppliers lower their development costs, reduce their time to market and simplify their certification to DO-254/ED-80 and DO-178C/ED-12C.

Existing and new use cases in the avionics segment are driving the need for new and innovative solutions to solve the underlying technical challenges as well as providing a robust path to the highest levels of safety certification. The 13th Gen Intel® Core™ processors bring a new paradigm with hybrid performance architecture allowing developers increased flexibility in their hardware designs. The CoreAVI software stack ported to Intel® Core™ processors enables system developers to quickly implement an open standard based, performant interface with the SoC for any graphics or compute application requiring safety certification to the highest assurance levels.

Learn More

CoreAVI

13th Gen Intel® Core™ Processors

References

[1] Intel®. "Introduction to Intel® performance hybrid architecture and Optimizations for IoT Use Case." Item number: 702965. December 2021

[2] RTCA DO-254/EUROCAE ED-80, Design Assurance Guidance for Airborne Electronic Hardware

[3] RTCA DO-178C/EUROCAE ED-12C, Software Considerations in Airborne Systems and Equipment Certification

[4]EASA "AMC 20-193 Use of multi-core processors" (Amendment 23, Subpart A General of "General Acceptable Means of Compliance for Airworthiness of Products, Parts and Appliances (AMC- 20)") Accessed on December 12 2022 from AMC-20

[5] Khronos Group Vulkan® SC™

[6] IEC 61508

[7] OpenGL®

[8] Certification Authorities Software Team (CAST)

Position Paper CAST-32A Multi-core Processors

November 2016 (Rev 0)

[9] Intel® Time Coordinated Computing (Intel® TCC)

Notices & Disclaimers

Intel technologies may require enabled hardware, software or service activation.

No product or component can be absolutely secure.

Customer is responsible for safety of the overall system, including compliance with applicable safety-related requirements or standards.

Your costs and results may vary.

This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.